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Results 1 - 20 of 200 Result page: 1 2 3 4 5 6 7 8 9 Best 200 shown 1 Profile-based optimizations: Reality-based optimization Scott McFarling March 2003 Proceedings of the international symposium on Code generation and runtime optimization Full text available: pdf(1.09 MB) Publisher Site Additional Information: full citation, ab Profile-based optimization has been studied extensively. Numerous papers an improvements. However, most of these papers have been limited to either brenchen performance. Also, most of these papers have looked at small applications with training scenarios. In this paper, we look at real use of large real-world desktoronsumption and disk performance are the primar
2 Systematic Power-Performance Trade-Off in MPEG-4 by Means of Selectic Address Optimization Opportunities M. Palkovic, M. Miranda, F. Catthoor March 2002 Proceedings of the conference on Design, automation and test in Full text available: pdf(116.86 kB) Publisher Site The hierarchical structure of real-life data dominated applications limits the experimisations. This limitation is often overcome by func-tioninlining. However, which causes a significant growth of instruction cachemisses and thus perform confirmed on experiments with our applications. We have developed a novel in inlining steered by cost/gain balance to trade-off

Near-optimal intraprocedural branch alignment

Cliff Young, David S. Johnson, Michael D. Smith, David R. Karger

May 1997 ACM SIGPLAN Notices, Proceedings of the ACM SIGPLAN 1997 conference and implementation, Volume 32 Issue 5

Full text available: pdf(1.56 MB)

Additional Information: full citation, abstract; references, ci

Branch alignment reorders the basic blocks of a program to minimize pipeline instructions. Prior work in branch alignment has produced useful heuristic met algorithm that usually achieves the minimum possible pipeline penalty and or of a provable optimum. We compare the control penalties and running times capproach and observe that both the greedy method an ...

4 Temperature-aware microarchitecture: Modeling and implementation Kevin Skadron, Mircea R. Stan, Karthik Sankaranarayanan, Wei Huang, Sivakun March 2004 ACM Transactions on Architecture and Code Optimization (TACO),

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Additional Information: full citation, abstract, references, citi

With cooling costs rising exponentially, designing cooling solutions for worst-c expensive. Chips that can autonomously modify their execution and power-dis of lower-cost cooling solutions while still guaranteeing safe temperature regul dynamic thermal management (DTM), however, requires a thermal model tha studies. This paper describes HotSpo ...

Keywords: Dynamic compact thermal models, dynamic thermal management, control, fetch gating

TRIPS: A polymorphous architecture for exploiting ILP, TLP, and DLP Karthikeyan Sankaralingam, Ramadass Nagarajan, Haiming Liu, Changkyu Kim, Burger, Stephen W. Keckler, Robert G. McDonald, Charles R. Moore March 2004 ACM Transactions on Architecture and Code Optimization (TACO), Full text available: pdf(832.30 KB)

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This paper describes the *polymorphous* TRIPS architecture that can be configured of parallelism. The TRIPS architecture is the first in a class of post-RISC, data data-graph execution (EDGE). This EDGE ISA is coupled with hardware mechand the on-chip memory system to be configured and combined in different methread-level parallelism. To adapt ...

Keywords: Computer architecture, configurable computing, scalable and high-

Papers: The lookahead strategy for distance-based location tracking in wire I-Fei Tsai, Rong-Hong Jan

October 1999 ACM SIGMOBILE Mobile Computing and Communications Review, Full text available: pdf(1.27 M8) Additional Information: full citation, abstract, referen

Based on a multi-scale, straight-oriented mobility model, this paper presents location tracking so the rate of location update can be reduced without incurri linear mobility graphs, the optimal registered cell is found by an iterative algo maximized. For planar mobility graphs, the authors employ the results from li registered cell. Performance gain i ...

7 Aggressive inlining

Andrew Ayers, Richard Schooler, Robert Gottlieb

May 1997 ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1997 conference and implementation, Volume 32 Issue 5

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Additional Information: full citation, abstract, references, ci

Existing research understates the benefits that can be obtained from inlining a profile information. Our implementation of inlining and cloning yields excellen lowers performance. We believe our good results can be explained by a numbintermediate-code level removes most technical restrictions on what can be in and incorporate profile information enables ...

8 Datapath and control for quantum wires

Nemanja Isailovic, Mark Whitney, Yatish Patel, John Kubiatowicz, Dean Copsey, Mark Oskin

March 2004 ACM Transactions on Architecture and Code Optimization (TACO),
Full text available: pdf(476.83 KB) Additional Information: full citation, abstract, reference

As quantum computing moves closer to reality the need for basic architectura Quantum wires, which transport quantum data, will be a fundamental compon architectures. Since they cannot consist of a stream of electrons, as in the cla fundamentally be designed differently. In this paper, we present two quantum swapping of adjacent qubits, and a teleportation wire, ...

Keywords: Architecture, Control, Layout

9 Software profiling for hot path prediction: less is more

Evelyn Duesterwald, Vasanth Bala

November 2000 Proceedings of the ninth international conference on Architectural operating systems, Volume 34, 28 Issue 5, 5

Full text available: pdf(286.07 KB)

Additional Information: full citation, abstract, references,

Recently, there has been a growing interest in exploiting profile information ir compilers, dynamic optimizers and, binary translators. In this paper, we show schemes that provide highly accurate information in an offline setting are ill-s systems. We experimentally demonstrate that hot path predictions must be m cost of missed opportunity tha ...

Advanced design and modeling techniques: Optimal design of high fan-in nonlinear programming

Hsu-Wei Huang, Cheng-Yeh Wang, Jing-Yang Jou

January 2004 Proceedings of the 2004 conference on Asia South Pacific design aut fair 2004

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In this paper, a novel strategy for designing the heterogeneous-tree multiplex delay model by curve fitting and then formulate the heterogeneous-tree multi of optimization problem called mixed-integer nonlinear programming (MINLP) size in each stage, is introduced to improve the speed of the heterogeneous-treat can determine the multiplexer architec ...

¹¹ Future technologies: Timing, energy, and thermal performance of three-din Shamik Das, Anantha Chandrakasan, Rafael Reif

April 2004

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We examine the performance of custom circuits in an emerging technology kn By combining multiple device layers with a high-density inter-layer interconne expected to provide better timing and energy performance relative to a single circuit. In this paper, we show that by using our performance-driven design to dissipation of standard-cell circuits can ...

Keywords: 3-D IC, 3-D integration, energy, thermal optimization, timing

¹² GADGET: a toolkit for optimization-based approaches to interface and disp James Fogarty, Scott E. Hudson

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Recent work is beginning to reveal the potential of numerical optimization as and displays. Optimization-based approaches can often allow a mix of indeper blended in ways that would be difficult to describe algorithmically. While optim offer several potential advantages, further research in this area is hampered to paper presents GADGET, an experimental toolk ...

Keywords: display generation, layout algorithms, numerical optimization, perc

13 Server performance and scalability: A smart hill-climbing algorithm for appl Bowei Xi, Zhen Liu, Mukund Raghavachari, Cathy H. Xia, Li Zhang
May 2004 Proceedings of the 13th international conference on World Wide W
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The overwhelming success of the Web as a mechanism for facilitating informa business transactions has ledto an increase in the deployment of complex entrypically run on Web Application Servers, which assume the burden of managi memory management, database access, etc., required by these applications. Server depends heavily on appropriate configuration. Co ...

Keywords: automatic tuning, gradient method, importance sampling, simulate

14 Extending Path Profiling across Loop Backedges and Procedure Boundarie Sriraman Tallam, Xiangyu Zhang, Rajiv Gupta

March 2004 Proceedings of the international symposium on Code generation and runtime optimization

Full text available: pdf(416,54 KB)

Additional Information: full citation

Since their introduction, path profiles have been used toguide the application and performing instruction scheduling. However, for optimization and schedulin frequency counts of paths that extend across loop iterations and crossprocedur referred to asinteresting paths in this paper, account for over 75% of theflow Although the frequency counts of interesting paths can b ...

Keywords: path profiles, overlapping path profiles, profileguided optimization,

¹⁵ Placement techniques: FastPlace: efficient analytical placement using cell : a hybrid net model

Natarajan Viswanathan, Chris Chong-Nuen Chu

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In this paper, we present FastPlace -- a fast, iterative, flat placement algorithmastPlace is based on the quadratic placement approach. The quadratic approach minimization problem as a convex quadratic program, which can be solved eff However it suffers from some drawbacks. First, the resulting placement has a resulting total wirelength ...

Keywords: analytical placement, net models, standard cell placement

¹⁶ Advances in embedded software scheduling techniques: Pareto-optimizatic embedded systems

Peng Yang, Francky Catthoor

October 2003 Proceedings of the 1st IEEE/ACM/IFIP international conference on H synthesis

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Pareto-set-based optimization can be found in several different areas of embe task scheduling, where different task mapping and ordering choices for a targe performance/cost tradeoffs. To explore this design space at run-time, a fast as have modeled the problem as the well known Multiple Choice Knapsack Proble greedy heuristic for the run-time task scheduling. To ...

Keywords: Pareto optimization, embedded system, low-power, scheduling

¹⁷ Code scheduling: Phi-Predication for light-weight if-conversion

Weihaw Chuang, Brad Calder, Jeanne Ferrante

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Predicated execution can eliminate hard to predict branches and help to enabl current predication variants exist where the result update is conditional based predicate. However, conditional writing of a register creates a naming problem stall the issuing of instructions. This problem arises from potential multiple pr which is unresolved until the prior ...

¹⁸ A comparative study of static and profile-based heuristics for inlining Matthew Arnold, Stephen Fink, Vivek Sarkar, Peter F. Sweeney January 2000 ACM SIGPLAN Notices, Proceedings of the ACM SIGPLAN workshop and optimization, Volume 35 Issue 7

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In this paper, we present a comparative study of static and pro Our motivation for this study is to use the results to design the can for the Jalapeño dynamic optimizing compiler for Java [6]. approximation algorithm for the KNAPSACK problem as a comm " meta-algorithm" for the inlining heuristics studie performance results for an implementation of these inlinin ...

19 Database theory, technology and applications (DTTA): On the semantics at languages for NP search and optimization problems

E. Zumpano, S. Greco, I. Trubitsyna, P. Veltri

March 2004

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It has been shown that NP (decision, search and optimization) problems can b (Datalog with unstratified negation) queries under stable model semantics. Ar is often neither simple nor intuitive and, besides, DATALOG does not allow to expressive power. This paper analyzes the power of Datalog-like languages in problems. In more detail, in t ...

Keywords: datalog, deductive and logic databases, expressive power of query queries

²⁰ Positional adaptation of processors: application to energy reduction Michael C. Huang, Jose Renau, Josep Torrellas

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Hardware-Based Profiling: An Effective Technique for Profile-Driven Optimization (1996) (Make Corrections) (7 citations) Thomas M. Conte, Burzin Patel, Kishore N. Menezes, J. Stan Cox International Journal of Parallel Programming

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Abstract: Profile-based optimizations can be used for instruction scheduling, loop scheduling, data preloading, function in-lining, and instruction cache performance enhancement. However, these techniques have not been embraced by software vendors because programs instrumented for profiling run significantly slower, an awkward compile-run-recompile sequence is required, and a test input suite must be collected and validated for each program. This paper introduces hardware-based profiling that uses... (Update)

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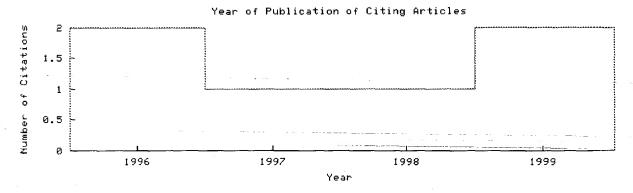
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